Overview
The process of developing appropriate verification environment for today's system-on-chip (SoC) designs becomes really hard, due to the fact that they include number of different protocols, peripherals, interfaces and processors. With such an increasing design complexity, verification tends to consume up to 60-80% project resources and often represents a bottleneck. Having all this in mind, thereusability in verification has a very significant role. In order to increase verification productivity, huge verification environments are assembled from a number of verification components. Each of the verification components is designed for a specific protocol or architecture and is configured by the environment to produce desired behavior.

eVCs are e-Language Verification Components used for verification environments based on VeriSity’s Specman-Elite tool. They are reusable, configurable, easy to use and integrate into different verification environments. Their development is based one Reuse Methodology (eRM) defined by VeriSity.

HyperTransport is a serial protocol used for chip-to-chip communication. It is a message based protocol with message based interrupt support and coherent/non coherent memory models. HyperTransport I/O link is nominally point-to-point link, but devices are allowed to have more than one link and form different topologies. HyperTransport eVC (HDH 1000) implements a HyperTransport protocol version 1.10. It can be used for verification of a device containing an interface for the HyperTransport I/O Link. It is developed as a fully eRM compliant eVC with standard structure and user interface. It is easy to configure and use. Multiple instances of HDH 1000 can be easily incorporated into a complex verification environment for apurpose of verifying a HyperTransport chain/tree architectures orSoC designs.

Features
- HyperTransport specification version 1.10
- Fully eRM compliant
- HyperTransport device types implemented: Host-Bridge, Tunnel, Cave, Bridge and Switch
- Support for direct packet routing
- Support for Error-Retry mode
- Support for optional Virtual Channels: Alternative, Stream and Non-Flow Controlled
- Support for 40-bit and 64-bit address remapping
- Support for Double-Hosted HyperTransport Chain configurations
- Built in link monitors for protocol checking
- Built in coverage analysis for all packet types
- HDL independent

Description
HyperTransport eVC (HDH 1000) implements the operation of a device with a single or multiple HyperTransport I/O Links (specification version 1.10). Depending on the number of HyperTransport links and their function in a HyperTransport chain, HyperTransport device can be a Host-Bridge, Cave, Tunnel, Bridge or Switch. HDH 1000 can be configured to model any of these device kinds by constraining fields of HDH 1000 environment.

HDH 1000 environment can have a function of:
- **Host-Bridge:** A component in a chain which performs chain initialization, configuration and defines an order of all link transactions in host-reflected traffic. Contains a single HyperTransport link.
- **Cave:** A component that ends a HyperTransport chain. Contains a single HyperTransport link.
- **Tunnel:** A component containing two HyperTransport links. It is capable of forwarding packets from one link to the other insuring that packets travel up and down the chain.
- **Bridge:** A component used for forming a HyperTransport tree, enabling the existence of subchains. Can have a tunneling capability. Bridge has multiple HyperTransport Links, one primary and none to multiple secondary ones.
- **Switch:** A component which enables complex HyperTransport configurations with multiple Host-Bridges and logical HyperTransport chains. Switch has multiple HyperTransport Links.
All HyperTransport devices are capable of initializing transactions on the link as well as responding to them.

HDH 1000 environment has a eRM standard structure with agents defining behavior of link interfaces. Each includes BFM s for signal driving and monitors with the ability to perform protocol checking on both, receive and transmit, traffic on the link. The behavior of HDH 1000 can easily be defined using sequences mechanism. On top of the HDH 1000 architecture there is functional coverage definition model with all relevant device configurations and traffic covered.

**Verification environments**

HyperTransport (HDH 1000) eVC environment can be used in module level verification. In those test environments, each DUT link interface is connected to a eVC link interface of appropriate kind. The example of a simple environment used for DUT Bridge Device verification is shown on figure below. Three HyperTransport eVC instances are used, one configured to be a HOST and the other two to be SLAVEs.

![Simple HyperTransport verification environment](image)

**Figure: Simple HyperTransport verification environment**

Multiple instances of a HyperTransport eVCs can be used in cooperation to verify a complex SoC designs such as HyperTransport trees and architectures with multiple HOSTs or multiple HyperTransport chains. Each of the instances can be configured to completely replace HDL component in chain/tree architecture. An example of a complex SoC verification environment is shown in the figure below.

![A more complex HyperTransport verification environment](image)

**Figure: A more complex HyperTransport verification environment**

Each of the devices in the environment shown on the figure above (HOSTs, SWITCHes, BRIDGEs, TUNNELs, CAVEs) can be a
HyperTransport eVC environment instance or a DUT device.

Applications

- Module level verification for a component with a HyperTransport Link interface.
- System On Chip level verification.

Deliverables

HyperTransport eVC is delivered in a form of a full eRM package containing:

- HDH 1000 encrypted code in e-Language
- Examples of eVC usage
- Demos for easy feature demonstration

Support

- One month of technical assistance via e-mail is included in the basic price
- The product can be customized according to the customer request
- Full technical support can be arranged
- Different license models

Availability

HyperTransport eVC (HDH 1000) will be available by the end of Q1/2004.

Contact Info

HDL Design House is fast growing privately owned company focused on providing re-usable, configurable and synthesizable VHDL/Verilog IP cores for SoC solutions and ASIC and FPGA design and design verification services.

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